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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,313	12/28/2001	Shunsuke Hirano	041-2082	4775

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EXAMINER

CHO, UN C

ART UNIT	PAPER NUMBER
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2682

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/028,313

Applicant(s)

HIRANO ET AL.

Examiner

Un C Cho

Art Unit

2682

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2,5 and 6.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2/3/2002, 1/9/2004 and 3/19/2004 was filed after the mailing date of the Application 10/028,313 on 12/28/2001. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

1. The disclosure is objected to because of the following informalities: Page 8, line 16 recites "divider 2" it should be divider 5 instead.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 9, 10 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Martin et al. (US 5,128,633).

Regarding claim 1, Martin teaches a multi-loop synthesizer comprising a voltage controlled oscillator (VCO, Fig. 1, 106, 126, 142) having a terminal for

oscillating a signal whose frequency corresponds to a control signal applied to the terminal; a loop divider (Fig. 1, 108, 130, 146) for dividing the frequency of the signal outputted from the voltage controlled oscillator so as to output a frequency divided signal having a divided frequency; a phase detector (Fig. 1, 102, 122, 138) detecting a phase of the frequency divided signal with that of a reference signal so as to output a difference signal representing a difference between the phase of the frequency divided signal and that of the reference signal; a loop filter (Fig. 1, 104, 124, 140) for smoothing the difference signal outputted from the phase detector so as to output the smoothed signal as the control signal to the terminal of the voltage controlled oscillator; a interstate divider (Fig. 1, 112, 128, 144) for dividing the frequency of the signal outputted from the voltage control oscillator so as to output a frequency divided signal having a divided frequency; and a mixer (Fig. 1, 110, 132) for mixing the frequency divided signal outputted from the interstate divider and the signal outputted from the voltage control oscillator so as to output a mixed signal (Martin, Col. 2, lines 29 – 48, Col. 3 lines 24 – 29 and 62 – 68).

Regarding claim 2, Martin teaches the interstate divider (Fig. 1, 112, 128, 144) comprises a second frequency divider for dividing the frequency of the signal outputted from the voltage control oscillator (Martin, Col. 2, lines 39 – 45).

Regarding claim 9, the claim is interpreted and rejected for the same reason as set forth in claim 1.

Regarding claim 10, the claim is interpreted and rejected for the same reason as set forth in claim 2.

Regarding claim 17, Martin teaches a communication device (Fig. 4, 400) installing therein the multi-loop frequency synthesizer (Martin, Col. 7, lines 60 – 62).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 8, 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Jokura (US 5,856,761).

Regarding claim 3, Martin teaches that the interstate divider (Fig. 1, 112, 128, 144) divides the frequency of the signal outputted from the voltage control oscillator (Fig. 1, 106, 126, 142). However, Martin fails to teach that the frequency divider divides on the basis of a frequency division ratio, said frequency divider being able to switch setting of the frequency division ratio. In contrast, Jokura teaches switching the frequency division ratio (Jokura, Col. 1, lines 56 – 58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Jokura to Martin to provide a PLL frequency synthesizer which is capable of high-speed channel switching without generating a high number of spurious signals in a large

capacity communication system with small channel intervals using high reference frequency.

Regarding claim 8, Martin fails to teach that the frequency division ratio is varied so as to set an average value from the temporally varied frequency division ratios to a desired frequency division ratio. However, Jokura teaches switching the frequency division ratio so as to set an average value from the switched frequency division ratios to a desired frequency division ratio (Jokura, Col. 1, lines 56 – 64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Jokura to Martin to provide a PLL frequency synthesizer which is capable of high-speed channel switching without generating a high number of spurious signals in a large capacity communication system with small channel intervals using high reference frequency.

Regarding claim 11, the claim is interpreted and rejected for the same reason as set forth in claim 3.

Regarding claim 16, the claim is interpreted and rejected for the same reason as set forth in claim 8.

6. Claims 4 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Lemay (CA 2,298,927).

Regarding claim 4, Martin teaches a frequency divider. However, Martin fails to teach that the first frequency divider comprises a pre-scalar for dividing

the frequency of the signal outputted from the voltage control oscillator and a third frequency divider connected therewith in series, said third frequency divider being adapted to divide an output signal outputted from the pre-scalar, said pre-scalar being served as the frequency division unit so as to supply the signal outputted from the pre-scalar to the mixer unit. In contrast, Lemay teaches a frequency divider (Fig. 2, 32) for dividing the frequency of the signal outputted from the voltage control oscillator (Fig. 2, 28) and another frequency divider (Fig. 2, 34) connected therewith in series, said frequency divider (Fig. 2, 34) adapted to divide an output signal outputted from the frequency divider (Fig. 2, 32) and said frequency divider (Fig. 2, 32) being served as the frequency division unit so as to supply the signal outputted from it to the mixer unit (Fig. 2, 30) (Lemay, Page 6, line 18 through Page 7, line 10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Lemay to Martin to provide a reliable and efficient circuit to attenuate oscillator frequency pulling including elimination of spurious and providing related harmonic isolation from the output of the voltage oscillator controller.

Regarding claim 12, the claim is interpreted and rejected for the same reason as set forth in claim 4.

7. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Tsukahara et al. (US 6,181,181).

Regarding claim 5, Martin teaches a mixer (Fig. 1, 110, 132). However, Martin fails to teach that the mixer unit has a first and a second phase shifter, a first and second mixer and an adder. In contrast, Tsukahara teaches a mixer circuit (Fig. 4, 211) comprising a first phase shifter (Fig. 4, 212) adapted to generate first and second signals, said first signal being shifted 90 degree away from the second signal; a second phase shifter (Fig. 4, 213) adapted to generate third and fourth signals, said third signal being shifted 90 degree away from the fourth signal; a first mixer (Fig. 4, 215) adapted to mix one of the first and second signals outputted from the first phase shifter and one of the third and fourth signals outputted from the second phase shifter; a second mixer (Fig. 4, 216) adapted to mix other of the first and second signals outputted from the first phase shifter and other of the third and fourth signals outputted from the second phase shifter; and an adder (Fig. 4, 217) adapted to add a mixed signal by the first and a mixed signal by the second mixer (Tsukahara, Col. 1, lines 55 through Col. 2, line 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Tsukahara to Martin to provide a phase shifter that obtains the two output signals in which the phase difference between the signals is substantially 90 degrees and has a small circuit area.

Regarding claim 16, the claim is interpreted and rejected for the same reason as set forth in claim 5.

8. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Yamagishi et al. (US 6,516,186).

Regarding claim 6, Martin teaches a mixer unit (Fig. 1, 110, 132).

However, Martin fails to teach that the mixer unit is served to be able to switch as an upconvert mixer and a downconvert mixer according to a control signal from an outside. In contrast, Yamagishi teaches that the frequency mixer (Fig. 10, 1 – 6) can be switched as an upconvert mixer and a downconvert mixer according to a local frequency signal from an outside (Yamagishi, Col. 1, lines 26 – 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Yamagishi to Martin to provide a new and improved image-rejection receiver, which can cancel an image signal completely.

Regarding claim 14, the claim is interpreted and rejected for the same reason as set forth in claim 6.

9. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin in view of Yamamoto et al. (US 6,006,078).

Regarding claim 7, Martin teaches an interstate divider (Fig. 1, 112, 128, 144). However, Martin fails to teach that the frequency division unit has a frequency division ratio, in which said frequency division ratio being a secured value. In contrast, Yamamoto teaches that the frequency division value M_i in the programmable divider (Fig. 1, 104) is changed by a program input from a controller in accordance with the frequency to be set when a reception frequency

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is changed so that the oscillating frequency of the VCO (Fig. 1, 103) can be arbitrarily changed by changing the frequency division value M_i (Yamamoto, Col. 1, lines 45 – 50). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Yamamoto to Martin to provide a receiver which is capable of reducing a period of time required for stabilizing a reception frequency at a desired frequency when the reception frequency is changed to the desired frequency.

Regarding claim 15, the claim is interpreted and rejected for the same reason as set forth in claim 7.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Un C Cho whose telephone number is (703)305-8725. The examiner can normally be reached on M ~ F 8:00AM to 4:30PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (703)308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Un C Cho
Examiner
Art Unit 2682

4/15/04 UC


LEE NGUYEN
PRIMARY EXAMINER